



US006455348B1

(12) **United States Patent**
Yamaguchi

(10) **Patent No.:** **US 6,455,348 B1**
(45) **Date of Patent:** **Sep. 24, 2002**

(54) **LEAD FRAME, RESIN-MOLDED SEMICONDUCTOR DEVICE, AND METHOD FOR MANUFACTURING THE SAME**

(75) **Inventor:** **Yukio Yamaguchi, Shiga (JP)**

(73) **Assignee:** **Matsushita Electric Industrial Co., Ltd., Osaka (JP)**

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/521,670**

(22) **Filed:** **Mar. 8, 2000**

Related U.S. Application Data

(62) Division of application No. 09/244,074, filed on Feb. 4, 1999, now Pat. No. 6,081,029.

(30) **Foreign Application Priority Data**

Mar. 12, 1998 (JP) 10-060811

(51) **Int. Cl.⁷** **H01L 21/44; H01L 21/48; H01L 21/50**

(52) **U.S. Cl.** **438/106; 438/108; 438/111; 438/112; 438/123; 438/124; 438/125; 257/666; 257/667; 257/676; 257/678**

(58) **Field of Search** **438/106-18, 613, 438/118, 119, 123-27; 257/666-675, 678**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,697,203 A * 9/1987 Sakai et al. 357/72
5,105,259 A 4/1992 McShane et al. 257/667
5,157,480 A 10/1992 McShane et al. 361/404
5,172,214 A 12/1992 Casto 257/676
5,225,897 A 7/1993 Reifel et al. 257/787
5,381,042 A 1/1995 Lerner et al. 257/712
5,521,429 A 5/1996 Aono et al. 257/676
5,641,987 A 6/1997 Lee 257/675
5,652,461 A 7/1997 Ootsuki et al. 257/675
5,731,632 A 3/1998 Kozono 257/717

5,834,691 A * 11/1998 Aoki 174/52.4
5,835,988 A 11/1998 Ishii 257/684
5,872,395 A * 2/1999 Fujimoto 257/675
5,900,676 A 5/1999 Kweon et al. 257/787
5,909,633 A * 6/1999 Haji et al. 438/612
5,920,115 A * 7/1999 Kimura et al. 257/668
5,929,511 A * 7/1999 Nakazawa et al. 257/666

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

JP	62-254457	11/1987	
JP	63-169753	7/1988	
JP	3-214763	9/1991	
JP	4-3450	1/1992	
JP	4-196574	7/1992	
JP	4-346256	* 12/1992	H01L/23/50
JP	7-297344	11/1995	
JP	8-46111	* 2/1996	H01L/23/50
JP	8-46125	* 2/1996	H01L/23/50
JP	8-51133	* 2/1996	H01L/21/66
JP	8-64625	* 3/1996	H01L/21/56
JP	09-232350	* 9/1997	H01L/21/56

Primary Examiner—Matthew Smith

Assistant Examiner—Granvill D Lee, Jr.

(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57)

ABSTRACT

A lead frame including signal-connecting leads, a die pad and support leads is provided. A semiconductor chip is bonded to the die pad with an adhesive. The semiconductor chip, electrode pads and the signal-connecting leads are electrically connected to each other with metal fine wires. And these members are encapsulated in a resin encapsulant. The back surface of the die pad is subjected to half etching or the like to form a convex portion and a flange portion surrounding the convex portion. Since a thin layer of the resin encapsulant exists under the flange portion, the resin encapsulant can hold the die pad more strongly and the moisture resistance of the device can be improved with the lower surface of the die pad protruding from the resin encapsulant. As a result, the characteristics of a resin-molded semiconductor device having a die pad exposed on the back surface of a resin encapsulant can be improved.

8 Claims, 15 Drawing Sheets

